

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

After entry of the foregoing amendment, Claims 1-7 are pending in the present application. Claim 1 is amended and Claims 6 and 7 are added without introduction of new matter.

In the outstanding Office Action, the drawings were objected to; the specification was objected to; Claims 1 and 4-5 were rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent No. 5,325,258 to Choi et al. (hereinafter "Choi"); and Claims 2 and 3 were rejected under 35 U.S.C. 103(a) as unpatentable over Choi.

Initially, Applicant's representatives thank Examiner Nguyen for granting the interview conducted on June 15, 2004. During the interview, differences between the claimed invention and the applied reference were discussed. The present response sets forth the substance of those discussions, including discussed amendments to independent Claim 1, which Examiner Nguyen agreed as showing the claimed invention to distinguish over the applied reference.

Regarding the objection to the drawings, Figure 4 is amended in view of the Examiner's comments. Accordingly, Applicant respectfully requests that the objection to the drawings be withdrawn.

Regarding the objection to the specification, the Title has been replaced in view of the Examiner's comments. Accordingly, Applicant respectfully requests that the objection to the title be withdrawn.

Addressing now the rejection of all claims under 35 U.S.C. 102(b) as anticipated by or unpatentable over Choi, summarized above, those rejections are respectfully traversed.

Amended Claim 1 is directed to a driving circuit which drives a semiconductor device based on a control signal supplied to a gate terminal. The driving circuit includes:

an overcurrent protection circuit configured to detect an overcurrent condition of said semiconductor device based on a sense voltage obtained from a sense electrode, and outputting an ***overcurrent protection signal to said gate terminal to instruct said semiconductor device to stop operating when an overcurrent condition is detected;***

an overcurrent protection signal masking part configured to output a masking signal invalidating said overcurrent protection signal during a masking period after a turn on and a turn off of said semiconductor device, and validating said overcurrent protection signal during periods other than said masking period; and

a control element configured to receive said masking signal and said overcurrent protection signal and configured to output said control signal.

Thus, as emphasized, the overcurrent protection signal instructs the semiconductor device to stop operating when an overcurrent condition is detected; and the separate masking signal invalidates the overcurrent protection signal during a masking period immediately after a turn on and turn off of the semiconductor device.

By way of background, during periods immediately after a semiconductor device is turned on or turned off, it is difficult to accurately detect an overcurrent condition due to imbalances between a sense voltage for detecting the overcurrent condition and the main current.¹ Filters and delay circuits can be used to prevent detection of an overcurrent condition during a period after turning on or turning off the semiconductor.² However, these background circuits have several drawbacks.³ The present invention is provided in view of those deficiencies.

In a non-limiting example, Figure 1 illustrates an embodiment of the present invention. The overcurrent protection circuit 6 compares a sense voltage V_{sense} to a detection threshold voltage V_{T1} , and outputs an overcurrent protection signal S6 based on that

¹ Specification, page 1, line 1 – page 2, line 9.

² Specification, page 2, lines 10-21.

³ Specification, page 2, lines 22 – page 3, line 4.

comparison.⁴ The masking circuit 5 receives a signal IN, which is synchronized with the turning on or off of the semiconductor. The signal IN charges the capacitor C12 and generates a voltage V9 for comparison against the reference voltage VR.⁵ The masking signal S5 is based on that comparison.⁶

Thus, an interruption control signal SC_OUT is output only if both the overcurrent protection signal S6 and masking signal S5 are received by the AND gate 25.⁷ Further, since the masking signal S5 is not output until charging of the capacitor C12, the masking signal S5 cannot validate the overcurrent protection signal immediately after the semiconductor device is turned on or off.⁸

The outstanding Office Action cites Choi as teaching the claimed overcurrent protection circuit and overcurrent protection signal masking part. More particularly, the Office Action cites the output of comparator 22 as teaching the overcurrent protection signal and the blanking stage 25 as teaching the masking circuit. However, as discussed during the interview, the blanking stage 25 *indiscriminately delays the output signal* of comparator 22 for 500 ns during all periods (i.e., masking or otherwise).⁹ Thus, the blanking stage 25 does not teach a masking signal that invalidates an output signal during a masking period and validates the same output signal during periods other than the masking period.

⁴ Specification, page 5, line 14 – page 6, line 1.

⁵ Specification, page 6, lines 11-22.

⁶ Specification, page 6, line 7- page 7, line 1.

⁷ Specification, page 7, lines 2-8.

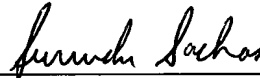
⁸ Specification, page 8, lines 4-13.

⁹ Choi, col. 4, line 58 – col. 5, line 2.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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